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SIMULATION AND COMPARATIVE ANALYSIS OF DIFFERENT TYPES OF MULTIPLIERS

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Abstract*— A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing system as well as in general processors. The various types of multipliers like Braun, Booth, Vedic, and Wallace Tree Multipliers are simulated using Hardware Description Language (HDL). The Simulated tool is Xilinx ISE 14.3. The major comparative analyses of these multipliers concentrate in number of LUT's and LUT-FF Pairs. This paper mainly reduces the area level of the Processors. And also checks with these Multipliers are done on FPGA Spartan 6 and Vertex 5 kits.

Keywords* — Braun, Booth, Vedic, Wallace Tree Multipliers, HDL Languages.

I. INTRODUCTION

The Multiplier main block is arithmetic unit. The number of addition operation is performed by a multiplier concept. The Braun Multiplier is a unsigned Multiplier. In this multiplier only use up to 16 bits. This Multiplier is also called as Carry Save Multiplier. The Booth Multiplier is multiplied with a both signed and unsigned numbers. The Multiplier design up to 32/64 bits. The Modified Booth Multiplier is also used to algorithmic level applications also. The next Vedic Multiplier is a Parallel multiplier; it is a Vertical Cross-wise Multiplier. This multiplier is fastest multiplier. This multiplier design up to 64 bits. . These types of multipliers are used in both Integer and Floating Point Multipliers. And the next multiplier is Tree Multiplier, Wallace tree. This multiplier is efficient one. These multipliers work under procedure steps, and also reduce the number of Partial Product of full adder and half adder. This design is up to 32 bits. These types of multipliers are concentrating in this project. The main aim of the project is reduce the area of the Processors [1][2]. The design concept up to this project is 4x4 multiplier structure only. The arrangement of Full adder and half adder is based on Hardware Description Language (HDL) coding style, the coding is written in Behavioural and Structural modelling. And also Register Transfer Level (RTL) Schematic model also shown in this paper. This type of comparison is used to done by Xilinx ISE 14.3 EDA tool. And also results are checks to FPGA Spartan 6 and Virtex 5 kits. .

This paper is organized as following. Section II Architecture of different types of multiplier structures and operations. Section III Simulation results and RTL schematic Structures, Comparative analysis in table forms are shown in Section IV, followed by the Conclusion in Section V.

II. ARCHITECTURE OF DIFFERENT TYPES OF MULTIPLIER STRUCTURES AND OPERATIONS

High-speed multiplication is another difficult function in a range of very large scale integration (VLSI) applications. Multiplication is logically carried out by a sequence of addition, subtraction and shifting operations, and Multiplications are expensive and slow operations. Multiplication is an important basic arithmetic operation and less common operation than addition, but it is still essential for microprocessors, digital signal processors. The multipliers are the structures where there will be many cascading stages of the full adder, so the performance of the full adders while cascading too many stages can be easily studied by analysing the power, delay, power-delay product of the different multipliers made from different adders [3].

2.1 Braun Multiplier

Braun multiplier is an parallel multiplier it is also called as carry save array multiplier, and it is easy to design one. The structure consists of array of AND gates and adders arranged in the iterative way and no need of logic registers. This can be called as non – addictive multipliers [4]. In the internal structure, each products can be generated in parallel with the AND gates, and each partial product can be added with the sum of partial product which has previously produced by using the row of adders.

The carry out will be shifted one bit to the left or right and then it will be added to the sum which is generated by the first adder and the newly generated partial product. The design of full adder using Braun Multiplier diagram shown in below Fig. 1. In the multiplier array a full adder with balanced carry and sum delays in desirable because the sum and carry signals are both in the critical path. The disadvantages of Braun multiplier is the number of components required in building

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blocks of Braun Multiplier increases quadratic ally with the number of bits. And the potential susceptibility to Glitching problems at the last stage of full adders due to exploitation of the Ripple Carry Adder (RCA).

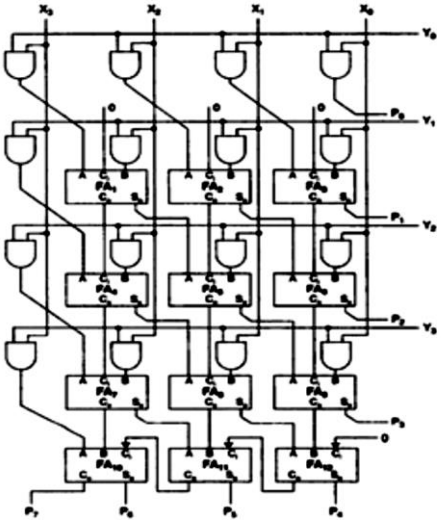

Fig 1: Architecture of 4x4 Braun Multiplier

2.2 Booth Multiplier

Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation.

Algorithm

1. The multiplicand and multiplier are placed in the m and Q registers respectively. A 1 bit register is placed logically to the right of the LSB (least significant bit) Q0 of Q register. This is denoted by Q-1. A and Q-1 are initially set to 0. Control logic checks the two bits Q0 and Q-1.

2. If the two bits are same (00 or 11) then all of the bits of A, Q, Q-1 are shifted 1 bit to the right. If they are not the same and if the combination is 10 then the multiplicand is subtracted from A and if the combination is 01 then the multiplicand is added with A. In both the cases results are stored in A, and after the addition or subtraction operation, A, Q, Q-1 are right shifted [5].

3. The shifting is the arithmetic right shift operation where the left most bit namely, A_{n-1} is not only shifted into A_{n-2} but also remains in A_{n-1}. This is to preserve the sign of the number in A and Q. The result of the multiplication will appear in the A and Q.

The Booth multiplier is multiplied two numbers, the numbers are either signed or unsigned numbers [6][7]. The Braun multiplier is used to multiply only the unsigned numbers; this is the one drawback of Braun multiplier. But booth multiplier multiply with both numbers.

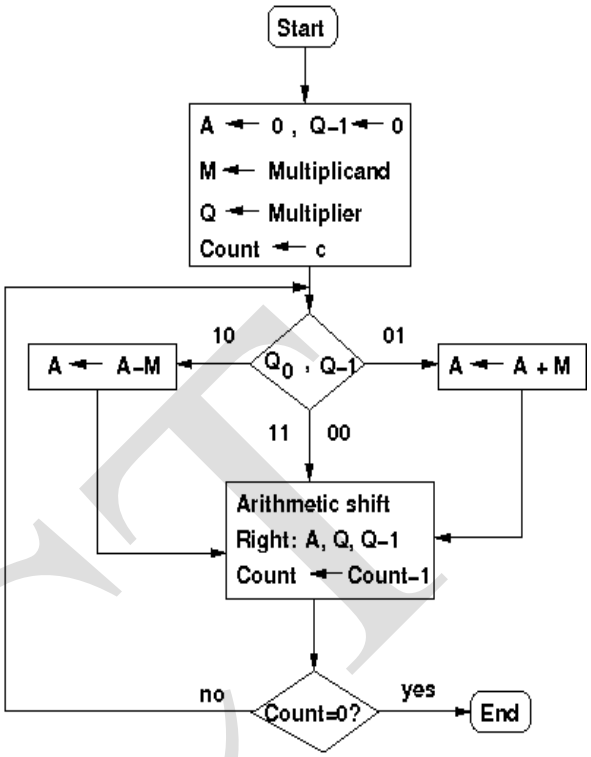

Fig 2 : Flow Chart of Booth Multiplier

2.3 Vedic Multiplier

Vedic Multiplier is a Vertical Crosswise structure; it generates all partial products and their sum in one step. Since the partial products and their sum are calculated in Parallel. The Vedic Multiplier is one of the fastest multiplier. The Vedic Multiplier works under Algorithmic basis [8][9].

Algorithm

1. Divided the Multiplicand A and Multiplicand B into two equal parts, each consisting of [N to (N/2) + 1] bits and [N/2 to 1] bits respectively, where first bit parts indicates the MSB and other represents LSB.
2.
3. Represents the parts of A as Am and Al and parts of B as Bm and Bl. Now represents A and B as Am Al and BmBl respectively.
4.
5. For example AXB we have general format as shown in below.

Am Al

Bm Bl

These inputs are multiplied with Vertical and Crosswise basis,

Am x Bm, Am x Bl, Al x Bl

Al x Bm

6. The individual multiplication products can be obtained by the partitioning method and applying the basic building blocks.

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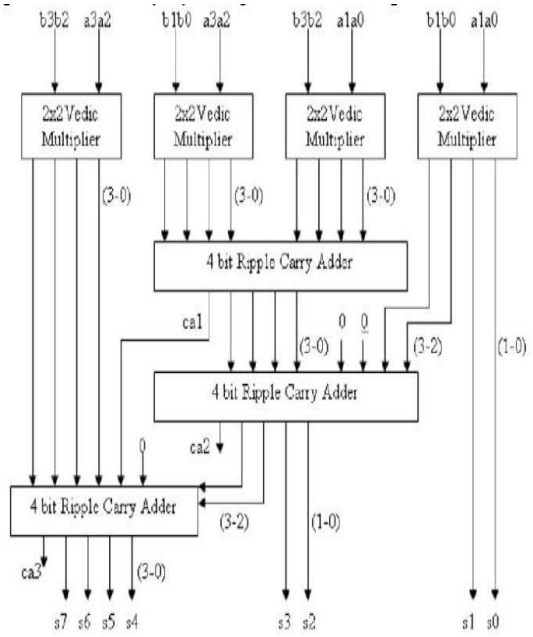

Fig 3: Architecture of 4x4 Vedic Multiplier

The Booth and Vedic Multipliers are used to many applications like Integer and Floating Point Multipliers and Calculations, Digital Signal Processors (DSPs) etc.,

2.4 Wallace Tree Multiplier

A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies two integer numbers. The Wallace tree multiplier has three steps to be followed,

- Multiply each bit of one of the arguments, by each bit of the other, yielding n^2 results.
- Reduce the number of partial products to two by layers of full and half adders.
- Group the wires in two numbers, and add them with a conventional adder.

The second section works as follows.

- Take any three wires with the same weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each three input wires.
- If there are two wires of the same weight left, input them into a half adder.
- If there is just one wire left, and connect it to the nextlayer.

The Wallace tree multiplier output structure is tee basis style, in this multiplier reduce the number of components and reduce the area.

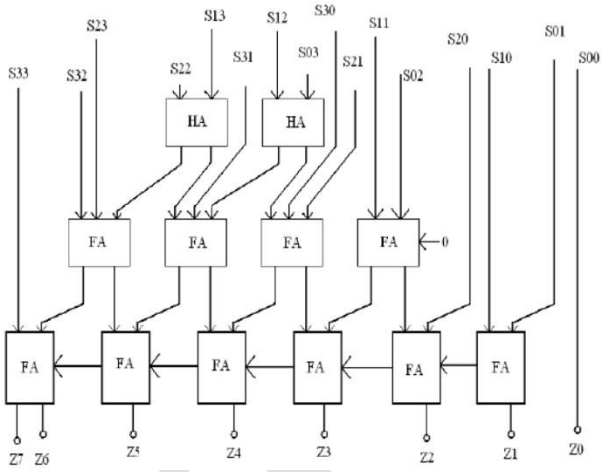

Fig 4 : Architecture of 4x4 Wallace Tree Multiplier

III. SIMULATION RESULAND RTL SCHEMATIC STRUCTURES

The simulation results are done by using Xilinx ISE 14.3 EDA tool, and VHDL programming is used. ISIM tool is used for Simulation process. Xilinx core generator tool is used to generate different types of multiplier core. The whole multiplier was tested against the Xilinx floating point multiplier core, and also check with FPGA Spartan 6, Virtex 5 kits. The Register Transfer Level (RTL) structures are generated by individual multipliers. These simulation results and schematic structures are shown in Fig. (5-12).

Fig 5 : 4x4 Braun Multiplier Output

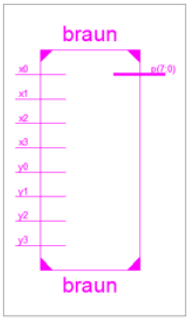

Fig 6 : RTL Schematic of 4x4 Braun Multiplier

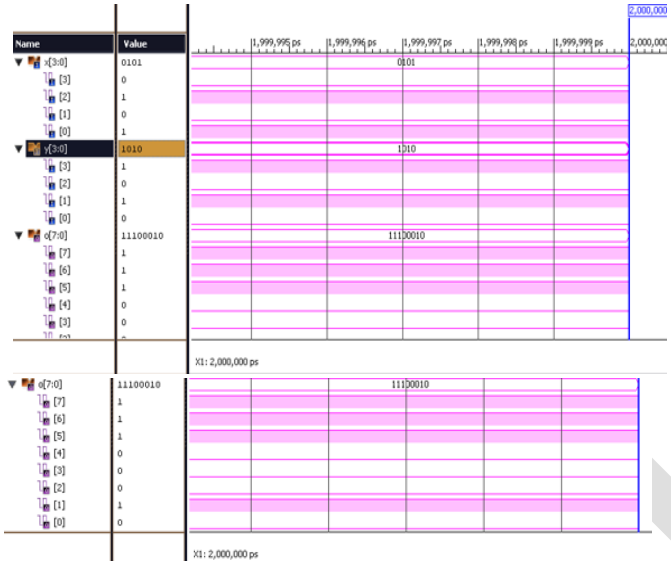

Fig 7 : 4x4 Booth Multiplier Output

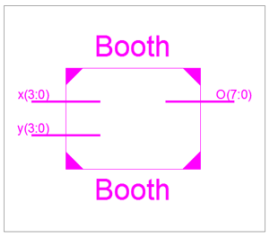

Fig 8 : RTL Schematic of 4x4 Booth Multiplier

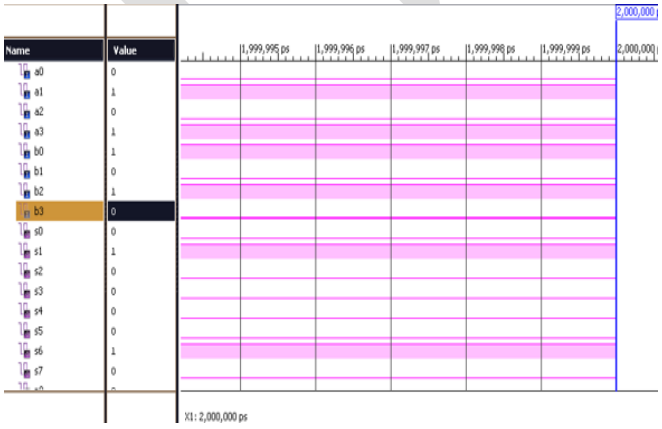

Fig 9 : 4x4 Vedic Multiplier Output

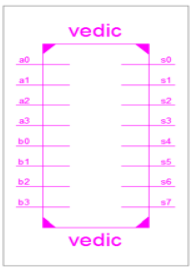

Fig 10 : RTL Schematic of 4x4 Vedic Multiplier

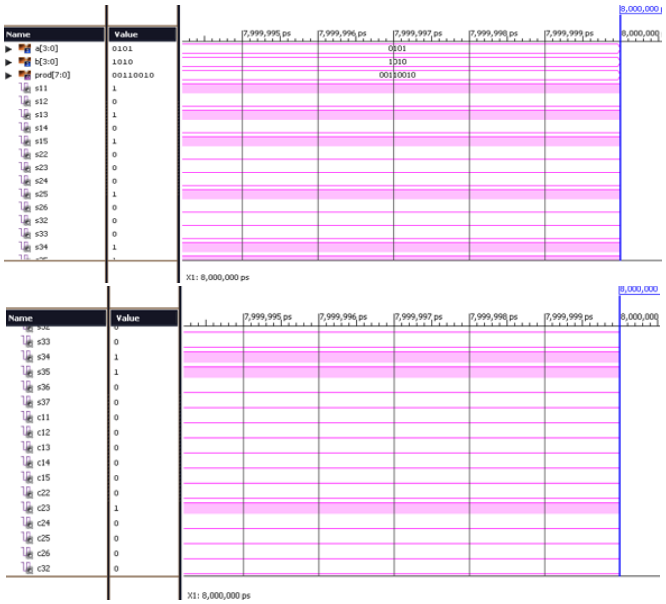

Fig 11 : 4x4 Wallace Tree Multiplier Output

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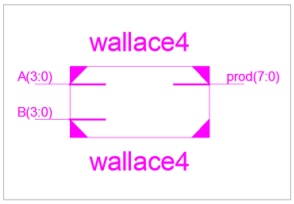

Fig 12 : RTL Schematic of 4x4 Wallace Tree Multiplier

IV. COMPARATIVE ANALYSIS OF DIFFERENT TYPES OF MULTIPLIERS

The comparison of Braun, Booth, Vedic, Wallace Tree Multiplier analysis shown in Table(1-4). The table shows major concerns on number of Slices LUT's and LUT-FF pairs.

Table 1: 4x4 Braun Multiplier

Logic Utilization	Used	Available	Utilization (Percentage)
No. of Slice LUT's	16	27288	1
No. of Fully Used LUT-FF Pairs	0	16	1
No. of Bonded IOB's	16	296	8

Table 2 : 4x4 Booth Multiplier

Logic Utilization	Used	Available	Utilization (Percentage)
No. of Slice LUT's	31	27288	2
No. of Fully Used LUT-FF Pairs	0	23	1
No. of Bonded IOB's	16	296	5

Table 3 : 4x4 Vedic Multiplier

Logic Utilization	Used	Available	Utilization (Percentage)
No. of Slice LUT's	24	27288	1
No. of Fully Used LUT-FF Pairs	0	24	2
No. of Bonded IOB's	16	296	6

Table 4 : 4x4 Wallace Tree Multiplier

Logic Utilization	Used	Available	Utilization (Percentage)
No. of Slice LUT's	23	27288	2
No. of Fully Used LUT-FF Pairs	0	23	2
No. of Bonded IOB's	16	296	5

V. CONCLUSION

The four types of Parallel Multipliers are used in many applications, likewise Braun, Vedic, Wallace tree multiplier supports for an unsigned numbers and Booth multiplier support for a both signed and unsigned numbers. The comparative analysis of this paper the Look-Up Tables (LUT's) and LUT-FF pairs are gradually decreasing of different types of multipliers, and also check with FPGA Spartan 6, Vertex 5. The future activities, these multipliers are used to design the increasing the number of bits an Integer and Floating Point Multipliers

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